

Socket No.: GR 98 P 2661

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By: M P

Date: August 16, 2002

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Manfred Engelhardt
Applic. No. : 09/816,923
Filed : March 23, 2001
Title : Integrated Circuit Configuration And Production Method
Examiner : Fernando Toledo - Art Unit: 2823

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INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. 1.97(c)

Hon. Commissioner of Patents and Trademarks,
Washington, D.C. 20231

Sir:

In accordance with 37 C.F.R. 1.97(c) copies of the following patents and/or publications are submitted herewith:

Published, European Patent Application No. EP 0 892 428 A2 (Nguyen et al.), dated January 20, 1999;

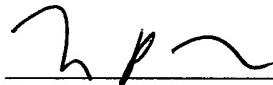
“A High Performance $3.97\mu\text{m}^2$ CMOS SRAM Technology Using Self-Aligned Local Interconnect and Copper Interconnect Metallization” (Woo et al.), 1998 Symposium on VLSI Technology Digest of Technical Papers, pp. 12-13;

“A High-Performance Sub-0.25 μm CMOS Technology with Multiple Thresholds and Copper Interconnects” (Su et al.), 1998 Symposium on VLSI Technology Digest of Technical Papers, pp. 18-19.

If no translation of pertinent portions of any foreign language patents or publications mentioned above is included with the aforementioned copies of those applications, patents and/or publications, it is because no existing translation is readily available to the applicant.

Consideration of this Information Disclosure Statement is requested in accordance with 37 C.F.R. 1.97(c). Enclosed is the IDS processing fee in the amount of \$180.00.

Respectfully submitted,



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For Applicants

Date: August 16, 2002

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